PIXEL INTERPOLATION CIRCUIT, PIXEL INTERPOLATION METHOD AND IMAGE

SCANNER

BACKGROUND OF THE INVENTION

5   Field of the Invention

This invention is related to an image processing method applied

to an image scanner using an image sensor, and particularly to

a method of generating interpolation pixel data for a digital image.

10   Description of the Related Art

In an image scanner using an image sensor, a pixel interpolation

process is performed to interpolate a lost pixel. Interpolation

pixel data is obtained by averaging pixel data neighboring the

lost pixel, or calculating a regression line of pixels neighboring

15   the lost pixel using a least-square method. Moreover, as described

in Japanese a Laid-Open Open Patent Publication 2003-101724, the

pixel interpolation data is also obtained by calculating a

biquadratic curve of four pixels neighboring the interpolation

pixel.

20   There are various methods for obtaining the interpolation

pixel data, however, a conventional pixel interpolation circuit

has a following problem. Since the conventional pixel interpolation

circuit calculates the interpolation pixel data using a fixed method

without considering an image characteristic, for example, a

25   difference between original pixels and interpolation pixels

(interpolation error) becomes large in an image area forming

outlines, and an image quality is deteriorated.

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The present invention has been made in order to solve above problems and to provide a pixel interpolation circuit, which is able to calculate an interpolation pixel data without causing the interpolation error for images having various characteristics.

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SUMMARY OF THE INVENTION

A pixel interpolation circuit according to this invention includes a plurality of interpolation circuits each calculating interpolation candidate data of a interpolation pixel and test 10 interpolation data of a plurality of pixels neighboring the interpolation pixel using different interpolation methods, a determining circuit for selecting one of the interpolation circuits based on a difference between the test interpolation data and actual pixel data and an output circuit for outputting the interpolation 15 candidate data calculated by the selected interpolation circuit as the interpolation pixel data.

A pixel interpolation method according to this invention comprising calculating interpolation candidate data of a interpolation pixel and test interpolation data of a plurality 20 of pixels neighboring the interpolation pixel, using different interpolation methods, selecting one of the interpolation methods based on a difference between the test interpolation data and actual pixel data, and outputting the interpolation candidate data calculated by the selected interpolation method as the interpolation 25 pixel data.

BRIEF DESCRIPTION OF DRAWINGS

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Fig. 1 is a block diagram illustrating a configuration of a pixel interpolation circuit according to this invention; Fig. 2 is a flow chart illustrating a process of a pixel interpolation calculation;

5   Fig. 3 is a diagram illustrating an example of test pixels;

Fig. 4 is a flow chart illustrating a calculation process of determination data;

Fig. 5 is a table illustrating a relation between the test pixels and the determination data;

10   Fig. 6 is a flow chart illustrating a calculation process of determination data;

Fig. 7 is a table illustrating a relation between interpolation circuits and the determination data;

Fig. 8 is a block diagram illustrating a configuration of a

15   pixel interpolation circuit according to the invention;

Fig. 9 is a diagram illustrating an example of original image data and input image data;

Fig. 10 is a diagram for explaining an interpolation calculation;

Fig. 11 is a diagram for explaining methods for calculating

20   test interpolation data and interpolation candidate data using a left/right averaging interpolation circuit;

Fig. 12 is a diagram for explaining methods for calculating test interpolation data and interpolation candidate data using a rightward up averaging interpolation circuit;

25   Fig. 13 is a table illustrating values of determination data M1 and M2;

Fig. 14 is a table illustrating values of evaluation data S1

and S2;

Fig. 15 is a block diagram illustrating a configuration of a pixel interpolation circuit according to the invention; Fig. 16 is a diagram illustrating an example of original image data and

5 input image data;

Fig. 17 is a diagram for explaining methods for calculating test interpolation data and interpolation candidate data using a leftward up averaging interpolation circuit;

Fig. 18 is a table illustrating values of determination data

10 M1 - M4;

Fig. 19 is a table illustrating values of evaluation data S1 - S3;

Fig. 20 is a table illustrating values of determination data M1 and M2; and

15 Fig. 21 is a table illustrating values of evaluation data S1 - S3.

Description of the Symbols

Preferred

20 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiment 1

Fig. 1 is a block diagram illustrating a configuration of a pixel interpolation circuit according to this invention. The pixel interpolation circuit illustrated in Fig. 1 includes a control

25 circuit 1, a determination circuit 2, an output circuit 3, and an interpolation unit 4. The interpolation unit 4 includes 1st-n^{th} interpolation circuits 4a-4n (n is an integer greater than 2),

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each of which performs different interpolation processes. Image data DI read by a scanner or a copy machine is sent to the determination circuit 2 and the interpolation unit 4. The image data DI sent to the interpolation unit 4, is sent to each of the 1st-n^{th} interpolation circuits 4a-4n. Fig. 2 is a flow chart illustrating a process of the pixel interpolation performed by the pixel interpolation circuit illustrated in Fig. 1.

Firstly, in the 1st interpolation circuit 4a, a test interpolation calculation is performed over pixels T1-Tm (hereinafter, referred to as test pixels) neighboring one of lost pixels included in the image data DI so as to calculate test interpolation data TD1[T1] - TD1[Tm] (Step 1).

Fig. 3 is a pattern diagram illustrating an example of lost pixels and test pixels. In Fig.3, lost pixels are represented with symbol "✕", and non-lost pixels are represented with symbol "◯". "L" is one of the lost pixels to be interpolated, and non-lost pixels T1 - Tm (m = 2 × k) neighboring the lost pixel are used as the test pixels. Fig. 3 (a) illustrates an example in which the non-lost pixels T1 - Tm located in left and right sides of the lost pixel L are used as the test pixels. Fig. 3 (b) illustrates an example in which non-lost pixels located in left and right sides of the lost pixel L in both vertical and horizontal directions are used as the test pixels.

The test interpolation calculation is performed by calculating interpolation pixel data for each of the test pixels on the assumption that the test pixels T1 - Tm are lost. For example, the test interpolation data TD1[T1] of the test pixel T1 is obtained by

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calculating an interpolation pixel data using the non-lost pixels neighboring the test pixel T1.

The test interpolation data TD1[T1] - TD1[Tm] (indicated as TD1 in Fig.1) calculated by the 1st interpolation circuit 4a is sent to the determination circuit 2. The determination circuit 2 calculates determination data M1[T1] - M1[Tm] that represent differences between the test interpolation data TD1[T1] - TD1[Tm] and data values DI[T1] - DI[Tm] of the test pixels T1-Tm (Step 2). The determination data M1[T1] - M1[Tm] is sent to the control circuit 1.

When the test interpolation data TD1[Tm] and the determination data M1[T1] - M1[Tm] are calculated for the last test pixel Tm (Step 3), the first interpolation circuit 4a performs an interpolation calculation over the lost pixel L, so as to calculate an interpolation candidate data D1 (Step 4). The interpolation candidate data D1 is sent to the output circuit 3.

The above-described processes of Step 1 - Step 4 are similarly performed in the 2nd-nth interpolation circuits 4b-4n (Step 5). In other words, the test interpolation data, TD2[T1] - TD2[Tm], ... TDn[T1] - TDn[Tm] (indicated as TD2 - TDn in Fig.1), are calculated in the 2nd-nth interpolation circuits 4b-4n and sent to the determination circuit 2. The determination circuit 2 calculates the determination data, M2[T1] - M2[Tm], ... Mn[T1] - Mn[Tm], for the test interpolation data TD2 - TDn. Then, interpolation candidate data D2 - Dn for the lost pixel L are calculated in the 2nd-nth interpolation circuits 4b-4n and send to the output circuit 3.

Fig. 4 is a flow chart illustrating a calculation process of

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the determination data in Step 2.

The determination circuit 2 calculates the absolute values of the differences between the test interpolation data TD1[T1] - TD1[Tm] and the values DI[T1] - DI[Tm] of the test pixels T1 - Tm (Step 21), respectively, and outputs the absolute values as the determination data M1[T1] - M1[Tm] (Step 22). The determination data M1[T1] - M1[Tm] are calculated using the following Formulas (1).

Formulas (1):

$$M1[T1] = |TD1[T1] - DI[T1]| \ldots M1[Tm] = |TD1[Tm] - DI[Tm]|$$

The determination circuit 2 also performs processes of Step 21 and Step 22 for the test interpolation data, TD2[T1] - TD2[Tm], … TDn[T1] - TDn[Tm], calculated by the 2nd-n^{th} interpolation circuits 4b-4n, so as to calculate the determination data M2[T1] - M2[Tm], … Mn[T1] - Mn[Tm].

Fig. 5 is a table representing all the determination data calculated by the determination circuit 2. As sown in Fig. 5, the determination data is calculated for each of the n×m test interpolation data of the test pixels T1 - Tm calculated by the 1st-n^{th} interpolation circuits 4a-4n.

Next, the determination data M1[T1] - M1[Tm], … Mn[T1] - Mn[Tm] are evaluated in the control circuit 1 (Step 6).

Fig. 6 is a flow chart illustrating a process of evaluating determination data in Step 6.

Firstly, the control circuit 1 calculates evaluation data S1 for the 1st interpolation circuit 4a by summing up the determination data M1[T1] - M1[Tm] (Step 61).

The control circuit 1 similarly calculates evaluation data S2

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- Sn for the $2^{nd}-n^{th}$ interpolation circuits 4b-4n (Step 62).

Calculations of the evaluation data S1 - Sn are represented by the following Formulas (2).

Formulas (2):

5    $S1 = M1[T1] + M1[T2] \ldots + M1[Tm]$

...

$Sn = Mn[T1] + Mn[T2] \ldots + Mn[Tm]$

Fig. 7 is a diagram showing relations between the $1^{st}-n^{th}$ interpolation circuits 4b-4n and the evaluation data S1 - Sn.

10   Next, the control circuit selects minimal evaluation data Sx from the evaluation data S1 - Sn (Step 63), and then specifies an interpolation circuit 4x corresponding to the evaluation data Sx (Step 64). The smaller a difference between the test interpolation data and actual image data is, the smaller the evaluation data

15   becomes. Therefore, the interpolation circuit 4x with the smallest evaluation data is estimated to have highest interpolation aptitude, which means the interpolation error becomes smallest. The control circuit 1 sends a selection signal C for selecting interpolation candidate data Dx calculated by the interpolation circuit 4x to

20   the output circuit 3 (Step 65).

The output circuit 3 selects the interpolation candidate data Dx according to the selection signal C, and outputs as interpolation data DO (Step 7).

The processes of Step 1 - Step 7 are performed for all the lost

25   pixels to calculate interpolation pixel data DO.

Fig. 8 is a block diagram illustrating a detailed configuration of the pixel interpolation unit 4 according to the invention.

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The interpolation unit 4 illustrated in Fig. 8 includes a left/right averaging interpolation circuit 5 and a rightward up averaging interpolation circuit 6.

Fig. 10 is a diagram for explaining an interpolation method of the left/right averaging interpolation circuit 5 and the rightward up averaging interpolation circuit 6. In Fig. 10, "L" represents a lost pixel to be interpolated by an interpolation calculation, and pixels "A"-"F" represent pixels neighboring the lost pixel L.

10   The left/right averaging interpolation circuit 5 calculates an average value XL of pixels B and E located in left and right sides of the lost pixel L, and the rightward up averaging interpolation circuit 6 calculates an average value of pixels D and C. The average values XL calculated by the left/right averaging interpolation

15   circuit 5 and the rightward up averaging interpolation circuit 6 are represented by the following Formulas (3) and (4), wherein data values (gradation values) of the pixels A- F are represented as XA - XF, respectively.

$XL = (XB + XE)/2$ ...Formula (3)

20    $XL = (XC + XD)/2$ ...Formula (4)

Fig. 9 is a pattern diagram illustrating an example of image data input into the interpolation circuit. In Figs. 9, non-lost pixels are represented with symbol "○" and symbol "●", and lost pixels are represented with symbol "✕". Fig. 9(a) illustrates

25   an original image, and Fig. 9 (b) illustrates a state in which pixels illustrated in a portion "LL" is lost. The original image in the lost portion LL represents a rightward up outline. The

gradation value of each of the pixels is represented by 8 bit (0 - 255) data, and pixels illustrated as "○" has a gradation value 255, and pixels illustrated as "●" has a gradation value 0.

Hereinafter, a process of calculating an interpolation pixel data of the lost pixel L illustrated in Fig. 9 (b) is explained. Here, as illustrated in Fig. 9 (b), pixels T1 - T4 each located in the left and right sides of the lost pixel L are used as the test pixels.

The left/right averaging interpolation circuit 5 calculates test interpolation data TD1[T1] - TD1[T4] for the test pixels T1 - T4 illustrated in Fig. 9 (b), using the Formula (3).

Fig. 11 is a diagram for explaining methods for calculating test interpolation data and interpolation candidate data using the left/right averaging interpolation circuit 5.

The test interpolation data TD1[T1] for the test pixel T1 is obtained by calculating the average value of pixels "T1B" and "T1E" located in left and right sides of the test pixel T1 as illustrated in Fig. 11 (a).

The test interpolation data TD1[T2] for the test pixel T2 is obtained by calculating the average value of pixels "T2B" and "T2E" located in left and right sides of the test pixel T2 as illustrated in Fig. 11 (b).

The test interpolation data TD1[T3] for the test pixel T3 is obtained by calculating the average value of pixels "T3B" and "T3E" located in left and right sides of the test pixel T3 as illustrated in Fig. 11 (c).

The test interpolation data TD1[T4] for the test pixel T4 is

obtained by calculating the average value of pixels "T4B" and "T4E" located in left and right sides of the test pixel T4 as illustrated in Fig. 11 (d).

Therefore, the test interpolation data TD1[T1] - TD1[T4] are calculated as follows;

$$TD1[T1] = (T1B + T1E) / 2 = (255 + 255) / 2 = 255$$

$$TD1[T2] = (T2B + T2E) / 2 = (255 + 0) / 2 = 127.5$$

$$TD1[T3] = (T3B + T3E) / 2 = (255 + 0) / 2 = 127.5$$

$$TD1[T4] = (T4B + T4E) / 2 = (0 + 0) / 2 = 0$$

As illustrated in Fig. 11 (e), the interpolation candidate data D1 is calculated by averaging pixels LB and LE on the left and right sides of the lost pixel L as follows;

$$D1 = (LB + LE) / 2 = (255 + 0) / 2 = 127.5$$

The determination circuit 2 obtains the determination data M1[T1] - M1[T4] by calculating the absolute values of the differences between the test interpolation data TD1[T1] - TD1[T4] and the values DI[T1] - DI[T4] of the test pixels T1 - T4.

The determination data M1[T1] - M1[T4] are calculated as follows.

$$M1[T1] = |TD1[T1] - DI[T1]| = |255 - 255| = 0$$

$$M1[T2] = |TD1[T2] - DI[T2]| = |127.5 - 255| = 127.5$$

$$M1[T3] = |TD1[T3] - DI[T3]| = |127.5 - 0| = 127.5$$

$$M1[T4] = |TD1[T4] - DI[T4]| = |0 - 0| = 0$$

The rightward up averaging interpolation circuit 6 calculates test interpolation data TD1[T1] - TD1[T4] for the test pixels T1 - T4 illustrated in Fig. 9 (b), using Formula (4).

Figs. 12 are diagrams for explaining methods for calculating test interpolation data and interpolation candidate data using

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the rightward up averaging interpolation circuit 6.

The test interpolation data TD2[T1] for the test pixel T1 is obtained by calculating the average value of pixels "T1D" and "T1C" located in upper right and lower left positions of the test pixel T1 as illustrated in Fig. 12 (a).

The test interpolation data TD2[T2] for the test pixel T2 is obtained by calculating the average value of pixels "T2D" and "T2C" located on the rightward up and leftward down positions of the test pixel T2 as illustrated in Fig. 12 (b).

The test interpolation data TD2[T3] for the test pixel T3 is obtained by calculating the average value of pixels "T3D" and "T3C" located on the rightward up and leftward down positions of the test pixel T3 as illustrated in Fig. 12 (c).

The test interpolation data TD2[T4] for the test pixel T4 is obtained by calculating the average value of pixels "T4D" and "T4C" located on the rightward up and leftward down positions of the test pixel T4 as illustrated in Fig. 12 (d).

Therefore, the test interpolation data TD1[T1] - TD1[T4] is calculated as follows;

TD2[T1] = (T1C + T1D) / 2 = (255 + 255) / 2 = 255

TD2[T2] = (T2C + T2D) / 2 = (255 + 0) / 2 = 127.5

TD2[T3] = (T3C + T3D) / 2 = (255 + 0) / 2 = 127.5

TD2[T4] = (T4C + T4D) / 2 = (0 + 0) / 2 = 0

As illustrated in Fig. 12 (e), the interpolation candidate data D2 is calculated by averaging pixels LD and LC located on the rightward up and leftward down positions of the lost pixel L as follows;

D2 = (LC + LD) / 2 = (0 + 0) / 2 = 0

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The determination circuit 2 obtains the determination data M2[T1] - M2[T4] by calculating the absolute values of the differences between the test interpolation data TD2[T1] - TD2[T4] and the values DI[T1] - DI[T4] of the test pixels T1 - T4.

The determination data M2[T1] - M2[T4] is calculated as follows;

M2[T1] = |TD2[T1] - DI[T1]| = |255 - 255| = 0

M2[T2] = |TD2[T2] - DI[T2]| = |127.5 - 255| = 127.5

M2[T3] = |TD2[T3] - DI[T3]| = |0 - 0| = 0

M2[T4] = |TD2[T4] - DI[T4]| = |0 - 0| = 0

Fig. 13 is a table showing values of determination data M1 and M2 of the test pixels T1 - T4 calculated as described above.

The control circuit 1 adds up the determination data M1[T1] - M1[T4], and calculates the evaluation data S1 for evaluating the interpolation aptitude of the left/right averaging interpolation circuit 5.

The evaluation data S1 is given as follows;

S1 = M1[T1] + M1[T2] + M1[T3] + M1[T4]

  = 0 + 127.5 + 127.5 + 0 = 255

In a similar way, the control circuit 1 adds up the determination data M2[T1] - M2[T4], and calculates the evaluation data S2 for evaluating the interpolation aptitude of the rightward up averaging interpolation circuit 6.

The evaluation data S2 is given as follows;

S2 = M2[T1] + M2[T2] + M2[T3] + M2[T4]

  = 0 + 127.5 + 0 + 0 = 127.5

Fig. 14 is a table showing the evaluation data S1 of the left/right averaging interpolation circuit 5 and the evaluation data S2 of

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the rightward up averaging interpolation circuit 6. As illustrated in Fig. 14, the evaluation data S2 of the rightward up averaging interpolation circuit 6 has the smallest value. As described above, the smaller the difference between the test interpolation data and actual image data is, the smaller the evaluation data becomes. Because the original image data illustrated in Fig. 9 (a) has a rightward up outline, the rightward up averaging interpolation circuit 6 is estimated to have the highest interpolation aptitude. The evaluation data shown in Fig. 14 also indicates that the rightward up averaging interpolation circuit 6 has the highest interpolation aptitude.

The control circuit 1 selects the evaluation data S2, and specifies the rightward up averaging calculating circuit 6 corresponding to this evaluation data. The control circuit 1 sends the selection signal C for selecting the interpolation candidate data D2 for the lost pixel L calculated by the rightward up averaging interpolation circuit 6 to the output circuit 3.

According to the selection signal C, the output circuit 3 outputs the interpolation candidate data D2 (D2 = 0) calculated by the rightward up averaging interpolation circuit 6 as the interpolation pixel data DO (DO = 0).

As illustrated in Figs. 9, a data value of the lost pixel L in the original image is 0, which means that the interpolation candidate data D2 (D2 = 0) calculated by the rightward up averaging interpolation circuit 6 has smaller error than the interpolation candidate data D1 (D1 = 127.5) calculated by the left/right averaging interpolation circuit 5.

As described above, by selecting the interpolation candidate data calculated by the different interpolation methods, based on the results of the test interpolation calculations, the interpolation pixel data can be accurately calculated using the most suitable interpolation method in accordance with an outline neighboring the interpolation pixel.

Embodiment 2

Fig. 15 is a block diagram illustrating another configuration of the interpolation unit 4. The interpolation unit 4 of the pixel interpolation circuit illustrated in Fig. 1 includes a left/right averaging interpolation circuit 5, a rightward up averaging interpolation circuit 6, and a leftward up averaging interpolation circuit 7. The left/right averaging interpolation circuit 5 and the rightward up averaging interpolation circuit 6 calculate the test interpolation data and the interpolation candidate data using the methods described in the Embodiment 1.

The leftward up averaging interpolation circuit 7 calculates average values of pixels located on the leftward up and rightward down positions of a pixel to be interpolated. In other words, the circuit calculates the average value "XL" of pixels "A" and "F" located on the leftward up and rightward down positions of the pixel L. The average value XL calculated by the leftward up averaging interpolation circuit 7 is represented by the following Formula (5), wherein data values (gradation values) of pixels A and F are represented as XA and XF, respectively.

$$XL = (XA + XF)/2 \dots \text{Formula (5)}$$

Fig. 16 is a pattern diagram illustrating another example

of image data input into the interpolation circuit. In Figs. 16, non-lost pixels are represented with symbol "○" and symbol "●", and lost pixels are represented with symbol "✕". Fig. 16 (a) illustrates an original image, and Fig. 16 (b) illustrates a state

. 5   in which pixels illustrated in a portion "LL" is lost. The original image in the lost portion LL represents a leftward up outline. The gradation value of each of the pixels is represented by 8 bit (0 - 255) data, and pixels illustrated as "○" has a gradation value 255, and pixels illustrated as "●" has a gradation value 0.

10   Hereinafter, processes of calculating interpolation pixel data of the lost pixel L illustrated in Fig. 16 (b) are explained. Here, as illustrated in Fig. 16 (b), pixels T1 - T4 each located in the left and right sides of the lost pixel L are used as the test pixels.

15   The leftward up averaging interpolation circuit 7 calculates test interpolation data TD3[T1] - TD3[T4] for the test pixels T1 - T4 illustrated in Fig. 16 (b), using the Formula (5).

Fig. 17 is a diagram for explaining methods for calculating the test interpolation data and the interpolation candidate data

20   using the leftward up averaging interpolation circuit 7.

The test interpolation data TD3[T1] for the test pixel T1 is obtained by calculating the average value of pixels "T1A" and "T1F" located on the leftward up and rightward down positions of the test pixel T1 as illustrated in Fig. 17 (a).

25   The test interpolation data TD3[T2] for the test pixel T2 is obtained by calculating the average value of pixels "T2A" and "T2F" located on the leftward up and rightward down positions of the

test pixel T2 as illustrated in Fig. 17 (b).

The test interpolation data TD3[T3] for the test pixel T3 is obtained by calculating the average value of pixels "T3A" and "T3F" located on the leftward up and rightward down positions of the test pixel T3 as illustrated in Fig. 17 (c).

The test interpolation data TD3[T4] for the test pixel T4 is obtained by calculating the average value of pixels "T4A" and "T4F" located on the leftward up and rightward down positions of the test pixel T4 as illustrated in Fig. 17 (d).

Therefore, the test interpolation data TD3[T1] - TD3[T4] are calculated as follows;

TD3[T1] = (T1A + T1F) / 2 = (255 + 255) / 2 = 255

TD3[T2] = (T2A + T2F) / 2 = (255 + 0) / 2 = 127.5

TD3[T3] = (T3A + T3F) / 2 = (0 + 0) / 2 = 0

TD3[T4] = (T4A + T4F) / 2 = (0 + 0) / 2 = 0

As illustrated in Fig. 17 (e), the interpolation candidate data D3 is calculated by averaging pixels LA and LF located on the leftward up and rightward down positions of the lost pixel L as follows;

D3 = (LA + LF) / 2 = (0 + 0) / 2 = 0

The determination circuit 2 obtains the determination data M1[T1] - M1[T4] by calculating the absolute values of the differences between the test interpolation data TD3[T1] - TD3[T4] and the values DI[T1] - DI[T4] of the test pixels T1 - T4.

The determination data M3[T1] through M3[T4] can be calculated as follows;

M3[T1] = |TD3[T1] - DI[T1]| = |255 - 255| = 0

M3[T2] = |TD3[T2] - DI[T2]| = |127.5 - 255| = 127.5

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M3[T3] = |TD3[T3] - DI[T3]| = |0 - 0| = 0

M3[T4] = |TD3[T4] - DI[T4]| = |0 - 0| = 0

The left/right averaging interpolation circuit 5 and the rightward up averaging interpolation circuit 6 calculate the interpolation candidate data D1 and D2 and the test interpolation data TD1[T1] - TD1[T4] and TD2[T1] - TD21[T4], and the determination circuit 2 calculates determination data M1[T1] - M1[T4] and M2[T1] - M2[T4] based on the test interpolation data. The processes in the left/right averaging interpolation circuit 5 and the rightward up averaging interpolation circuit 6 are described in the Embodiment 1.

Here, the interpolation candidate data D1 calculated by the left/right averaging interpolation circuit 5 is 127.5, and the interpolation candidate data D2 calculated by the rightward up averaging interpolation circuit 6 is 127.5.

Fig. 18 is a table showing values of determination data M1, M2, and M3 for test pixels T1 - T4.

The control circuit 1 adds up the determination data M1[T1] - M1[T4], and calculates the evaluation data S1 for evaluating the interpolation aptitude of the left/right averaging interpolation circuit 5.

The evaluation data S1 is given as follows;

S1 = M1[T1] + M1[T2] + M1[T3] + M1[T4]

= 0 + 127.5 + 127.5 + 0 = 255

In a similar way, the control circuit 1 adds up the determination data M2[T1] - M2[T4], and calculates the evaluation data S2 for evaluating the interpolation aptitude of the rightward up averaging interpolation circuit 6

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The evaluation data S2 is given as follows;

$$S2 = M2[T1] + M2[T2] + M2[T3] + M2[T4]$$

$$= 127.5 + 127.5 + 127.5 + 0 = 382.5$$

In a similar way, the control circuit 1 adds up the determination data M3[T1] – M3[T4], and calculates the evaluation data S3 for evaluating the interpolation aptitude of the leftward up averaging interpolation circuit 7.

The evaluation data S3 is given as follows;

$$S3 = M3[T1] + M3[T2] + M3[T3] + M3[T4]$$

$$= 0 + 127.5 + 0 + 0 = 127.5$$

Fig. 19 is a table showing values of the evaluation data S1, S2 and S3, which are calculated for the left/right averaging interpolation circuit 5, the rightward up averaging interpolation circuit 6, and the leftward up averaging interpolation circuit 7. As illustrated in Fig. 19, the evaluation data S3 of the leftward up averaging interpolation circuit 7 has a smallest value. As described above, the smaller the difference between the test interpolation data and actual image data is, the lower the evaluation data becomes. Because the original image data illustrated in Fig. 16 (a) has a rightward up outline, the leftward up averaging interpolation circuit 7 is estimated to have the highest interpolation aptitude. The evaluation data represented in Fig. 19 also indicates that the leftward up averaging interpolation circuit 7 has the highest interpolation aptitude.

The control circuit 1 selects the minimal evaluation data S3, and specifies leftward up averaging interpolation circuit 7 corresponding to this evaluation data. The control circuit sends

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the selection signal C for selecting the interpolation candidate data D3 calculated by the leftward up averaging interpolation circuit 7 for the lost pixel L to the output circuit 3.

According to the selection signal C, the output circuit 3 outputs the interpolation candidate data D3 (D3 = 0) calculated by the leftward up averaging interpolation circuit 7 as the interpolation pixel data DO (DO = 0).

As illustrated in Figs. 16, a data value of the lost pixel L in the original image is 0, which means that the interpolation candidate data D3 (D3 = 0) calculated by the leftward up averaging interpolation circuit 7 has smaller error than the interpolation candidate data D1 (D1 = 127.5) calculated by the left/right averaging interpolation circuit 5 or the interpolation candidate data D2 (D2 = 127.5) calculated by the rightward up averaging interpolation circuit 6.

As described above, by further providing the leftward up averaging interpolation circuit 7, more accurate interpolation process can be realized. In other words, the most suitable interpolation method is used for an image having different characteristics. Furthermore, the pixel interpolation circuit according to this invention can be used for increasing the number of pixels of an input image.

In the interpolation unit 4, the interpolation candidate data may be calculated using methods other than a left/right averaging interpolation, a rightward up average interpolation, or a leftward up average interpolation. For example such a method as calculating interpolation pixel using the least-square method, or calculating interpolation pixel data using a biquadratic curve obtained from

four pixels neighboring the interpolation pixel can be used. In the pixel interpolation circuit according to this invention, various kinds of interpolation circuits can further be added to the interpolation unit 4 without drastically modifying a configuration of the whole circuit.

Embodiment 3

Data amount of the determination data to be processed in the determination circuit 2 may be increased when the number of the interpolation circuits composing the interpolation unit 4 is increased. The data amount of the determination data can be decreased, by binarizing or ternarizing the determination data using a predefined threshold value.

As an example, a method of ternarizing the determination data values will be explained.

The determination circuit 2 compares the absolute value of the difference between the test interpolation data $TD1[T1]$ calculated by the first interpolation circuit 4a and the value $DI[T1]$ of the test pixel T1, with two predefined threshold values TH1 and TH2 $(0 \leq TH1 < TH2)$. When the absolute value is smaller than the threshold value TH1, a value of the determination data $M1[T1]$ is set -1; when the absolute value is larger than the threshold value TH1 and smaller than the threshold value TH2, a value of the determination data is set 0; and when the absolute value is larger than the threshold value TH2, a value of the determination data is set 1.

That is:

if $0 \leq |TD1[T1] - DI[T1]| < TH1$,

$M1[T1] = -1$;

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if $TH1 \leq |TD1[T1] - DI[T1]| < TH2$,

$M1[T1] = 0$; and

if $TH2 \leq |TD1[T1] - DI[T1]|$,

$M1[T1] = 1$.

5   The determination circuit 2 similarly calculates the determination data $M1[T2] - M1[Tm]$ for the test pixels $T2 - Tm$. That is:

if $0 \leq |TD1[T2] - DI[T2]| < TH1$,

$M1[T2] = -1$;

10   if $TH1 \leq |TD1[T2] - DI[T2]| < TH2$,

$M1[T2] = 0$;

if $TH2 \leq |TD1[T2] - DI[T2]|$,

$M1[T2] = 1$;

...

15   if $0 \leq |TD1[Tm] - DI[Tm]| < TH1$,

$M1[Tm] = -1$;

if $TH1 \leq |TD1[Tm] - DI[Tm]| < TH2$,

$M1[Tm] = 0$; and

if $TH2 \leq |TD1[Tm] - DI[Tm]|$,

20     $M1[Tm] = 1$.

The determination data $M1[T1] - M1[Tm]$ calculated in the above described method represent error of the test interpolation data with three values, -1, 0, and 1. The determination data becomes -1 when the error is small.

25   The determination circuit 2 similarly calculates the ternarized determination data $MD2[T1] - MD2[Tm]$ for the test interpolation data $TD2[T1] - TD2[Tm]$, ... $TDn[T1] - TDn[Tm]$ calculated by the $2^{nd}-n^{th}$

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interpolation circuits 4b-4n.

Hereinafter, a process of calculating ternarized determination data in the pixel interpolation circuit illustrated in Fig. 8 will be explained. In the following explanation, the interpolation pixel data for the lost pixel L illustrated in Fig. 9 (b) will be calculated, and the threshold values TH1=50 and TH2=100 will be used.

As calculated in Embodiment 1, the absolute values of the differences between the test interpolation data TD1[T1] - TD1[T4] and the values DI[T1] - DI[T4] of the test pixels T1 - T4 are given as follows;

$$|TD1[T1] - DI[T1]| = |255 - 255| = 0$$

$$|TD1[T2] - DI[T2]| = |127.5 - 255| = 127.5$$

$$|TD1[T3] - DI[T3]| = |127.5 - 0| = 127.5$$

$$|TD1[T4] - DI[T4]| = |0 - 0| = 0$$

Relations between these absolute values and the threshold values TH1 (TH1 = 50) and TH2 (TH1 = 100) are shown as follows;

$$|TD1[T1] - DI[T1]| < TH1$$

$$TH2 \leq |TD1[T2] - DI[T2]|$$

$$TH2 \leq |TD1[T3] - DI[T3]|$$

$$|TD1[T4] - DI[T4]| < TH1$$

Therefore, the determination data calculated for the left/right averaging interpolation circuit 5 are given as follows;

$$M1[T1] = -1$$

$$M1[T2] = 1$$

$$M1[T3] = 1$$

$$M1[T4] = -1$$

The absolute values of the differences between the test

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interpolation data TD1[T1] - TD1[T4] calculated by the rightward up averaging interpolation circuit 6 and the values DI[T1] - DI[T4] of the test pixels T1 - T4 are given as follows;

$|TD2[T1] - DI[T1]| = |255 - 255| = 0$

$|TD2[T2] - DI[T2]| = |127.5 - 255| = 127.5$

$|TD2[T3] - DI[T3]| = |0 - 0| = 0$

$|TD2[T4] - DI[T4]| = |0 - 0| = 0$

Relations between these absolute values and the threshold values TH1 (TH1 = 50) and TH2 (TH1 = 100) are given as follows;

$|TD2[T1] - DI[T1]| < TH1$

$TH2 \leq |TD2[T2] - DI[T2]|$

$TH2 \leq |TD2[T3] - DI[T3]|$

$|TD2[T4] - DI[T4]| < TH1$

Therefore, the determination data calculated for the rightward up averaging interpolation circuit 6 are given as follows;

$M2[T1] = -1$

$M2[T2] = 1$

$M2[T3] = -1$

$M2[T4] = -1$

Fig. 20 is a table showing values of the ternarized determination data M1 and M2 for the test pixels T1 - T4.

The control circuit 1 adds up the ternarized determination data M1[T1]-M1[T4], and calculates the evaluation data S1 for the left/right averaging interpolation circuit 5.

The evaluation data S1 is given as follows;

$S1 = M1[T1] + M1[T2] + M1[T3] + M1[T4]$

$= (-1) + 1 + 1 + (-1)$

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= 0

Similarly, the control circuit 1 adds up the determination data M2[T1] - M2[T4], and calculates the evaluation data S2 for evaluating the rightward up averaging interpolation circuit 6.

The evaluation data S2 is given as follows;

$$S2 = M2[T1] + M2[T2] + M2[T3] + M2[T4]$$

$$= (-1) + 1 + (-1) + (-1)$$

$$= -2$$

Fig. 21 is a table showing the evaluation data S1 of the left/right averaging interpolation circuit 5 and the evaluation data S2 of the rightward up averaging interpolation circuit 6. As shown in Fig. 21, the evaluation data S2 calculated for the rightward up averaging interpolation circuit 6 has the smallest value. The smaller the difference between the test interpolation data and actual image data is, the smaller the evaluation data becomes. Because, the original image data illustrated in Fig. 9 (a) represents a rightward up outline, the rightward up average interpolation circuit 6 is estimated to have high interpolation aptitude. The evaluation data S2 has the smallest value as shown in Fig. 14, indicating that the interpolation aptitude of the rightward up averaging interpolation circuit 6 is high, which means the interpolation method can be properly selected even if the determination data is ternarized.

In the above explanation, the determination data is ternarized using two threshold values. The data volume of the determination data can be also decreased by binarizing them using one threshold value or by decreasing the number of bits.

The pixel interpolation circuit according to this invention may be configured by either hardware or software, or may be configured with both hardware and software being properly mixed.

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